SSDs with Error-Prediction LDPC (EP-LDPC) and Error-Recovery Schemes

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Outline

- Introduction
- Error Prediction (EP) LDPC scheme
  - Measurement results
- Error Recovery (ER) scheme
  - Program disturb error recovery pulse (PDRP)
  - Data retention error recovery pulse (DRRP)
- Summary & Conclusion
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• Introduction
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• Summary & Conclusion
NAND Controller Architecture

NAND Controller

Host I/F

Flash Translation Layer (FTL)
- Bad block management
- Address translation from logical address to physical address of NAND
- Wear-leveling
- Interleaving
- Error correcting code (ECC)

NAND I/F

NAND Controller Architecture

- Stronger ECC is required in the scaled NAND.
- Low-density-parity-check (LDPC) ECC is needed.

R. Motwani et al., Flash Memory Summit, 2011.
Inter-cell Coupling

- Floating gate (FG)-FG capacitive coupling significantly degrades memory cell reliability as the design rules shrink.
- Direct field effect to channel is also observed.

J-D. Lee et al., *EDL*, pp. 264-266, 2002.
Problem of Soft Decoding LDPC ECC

- Log-likelihood ratio is input to LDPC decoder.
- Increased number of $V_{\text{ref}}$ result in large seq. read cycle.

$$\text{LLR}(y) = \ln \frac{p(x = 0 \mid y)}{p(x = 1 \mid y)}$$

$x$: Original symbol

$y$: Received symbol

$V_{\text{TH}}$: Threshold voltage

$V_{\text{ref1}}$: Reference voltage 1

$V_{\text{ref2}}$: Reference voltage 2

Data state: “11” “01” “00” “10”

LLR: -8 -3 -1 +1 +3 +8

Very likely to be “0”

Very likely to be “1”

R. Motwani et al., *Flash Memory Summit*, 2011.
Objectives of This Work

• To propose an error prediction (EP) LDPC ECC scheme without sequential read cycle increase to realize high reliability.

• To propose error recovery (ER) scheme to further enhance reliability.
Proposed SSD Architecture

Program

Initial data

Host

Read

Yes

Error correction successful?

No

Error recovery sequencer

Proposed error recovery (ER) scheme

Proposed EP-LDPC architecture

Number of “1”s ($N_{1}^{"initial\"}$) counter

LDPC encoder

$N_{1}^{"initial\"}$ is added to the user data.

LDPC decoder

Error prediction unit

Error recovery pulses

Apply error recovery pulses.

$T_{Retention}$ table $N_{W/E}$ table EP table

Inter-cell coupling information

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Concept of the Proposed EP-LDPC

- $V_{TH}$ information (x3)
- Inter-cell coupling information
- Write/erase cycles ($N_{W/E}$)
- Retention time ($T_{Retention}$)

Less sequential read cycles

**BER_{Est}: Estimated BER with the error prediction sequence**

FIGURE:

**Conventional**

- $V_{ref1}$
- $V_{ref21}$

**Proposed**

- $V_{ref}$

**Likelihood of data “0”**

$LLR(0) = \log \frac{1 - BER_{Est}}{BER_{Est}}$

**Likelihood of data “1”**

$LLR(1) = \log \frac{BER_{Est}}{1 - BER_{Est}}$
Program Sequence of the EP LDPC

- To estimate BER of the lower pages, \( N_1 \) is counted and added to the program data.
- \( N_1 \) is protected by triplicated BCH ECC.

- Data transfer from the host
- Record \( N_{"1"} \) of the initial data \((N_{"1"}\text{initial})\)
- \( N_{"1"} \): Number of "1"-data
- Program data to NAND

<table>
<thead>
<tr>
<th>Initial data</th>
<th>Parity (LDPC)</th>
<th>Stored with BCH</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( N_{&quot;1&quot;} )</td>
<td>( N_{&quot;1&quot;} )</td>
</tr>
</tbody>
</table>
Overall BER Estimation

\[ \text{BER}_{\text{Lower}} = \left| N^{"1"}_{\text{measured}} - N^{"1"}_{\text{initial}} \right| / \text{(Page size)} \]

Data Retention Error: **Ejection** of electrons

<table>
<thead>
<tr>
<th># of cells</th>
</tr>
</thead>
<tbody>
<tr>
<td>Upper 1 1</td>
</tr>
<tr>
<td>Lower 1 1</td>
</tr>
</tbody>
</table>

Lower page data retention error: 0 → 1

Program Disturb Error: **Injection** of electrons

<table>
<thead>
<tr>
<th># of cells</th>
</tr>
</thead>
<tbody>
<tr>
<td>Upper 1 1</td>
</tr>
<tr>
<td>Lower 0 0</td>
</tr>
</tbody>
</table>

Lower page data retention error: 1 → 0
BER & Retention Time Estimation

- BER is estimated from the difference of the number of “1”-data.
- Retention time is estimated from the table (BER vs. retention time).

![Graph showing BER vs. Retention Time](image)

- Estimated BER
- Measured BER
- $N_{W/E}$: 2k cycles
- $N_{W/E}$: 5k cycles
- $N_{W/E}$: 10k cycles
- Estimated retention time
- @85 degC

Retention time, $T_{Retention}$ (Day)
Pre-recorded Tables (1)

$T_{\text{Retention}}$ table

<table>
<thead>
<tr>
<th>Retention time</th>
<th>$N_{W/E}$</th>
<th>$N_{W/E}$</th>
<th>..........</th>
<th>$N_{W/E}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Day 0</td>
<td>BER_0.0</td>
<td>BER_0.1</td>
<td>..........</td>
<td>BER_0.10</td>
</tr>
<tr>
<td>Day 1</td>
<td>BER_1.0</td>
<td>BER_1.1</td>
<td>..........</td>
<td>BER_1.10</td>
</tr>
<tr>
<td>Day 100</td>
<td>BER_{100}.0</td>
<td>BER_{100}.1</td>
<td>..........</td>
<td>BER_{100}.10</td>
</tr>
</tbody>
</table>

$N_{W/E}$ table (Also used for wear-leveling)

<table>
<thead>
<tr>
<th>Block number</th>
<th>0</th>
<th>1</th>
<th>..........</th>
<th>65536</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_{W/E}$</td>
<td>$N_{W/E0}$</td>
<td>$N_{W/E1}$</td>
<td>..........</td>
<td>$N_{W/E65536}$</td>
</tr>
</tbody>
</table>
Error Prediction

- Error prediction is performed with EP table.

\[
\text{BER}_{\text{Est}} \sim \frac{\text{BER}_{\text{Left } "01"} + \text{BER}_{\text{Right } "01"} + \text{BER}_{\text{Upper } "01"} + \text{BER}_{\text{Lower } "01"}}{4}
= \frac{0.0015 + 0.0015 + 0.0012 + 0.0013}{4} = 0.0014
\]
#### Pre-recorded Tables (2)

<table>
<thead>
<tr>
<th>Target cell data</th>
<th>Upper cell data</th>
<th>“11”</th>
<th>“01”</th>
<th>“00”</th>
<th>“10”</th>
</tr>
</thead>
<tbody>
<tr>
<td>“11”</td>
<td>BER₁ , BER₅</td>
<td>BER₉</td>
<td>BER₁₃</td>
<td></td>
<td></td>
</tr>
<tr>
<td>“01”</td>
<td>BER₂ , BER₆</td>
<td>BER₁₀</td>
<td>BER₁₄</td>
<td></td>
<td></td>
</tr>
<tr>
<td>“00”</td>
<td>BER₃ , BER₇</td>
<td>BER₁₁</td>
<td>BER₁₅</td>
<td></td>
<td></td>
</tr>
<tr>
<td>“10”</td>
<td>BER₄ , BER₈</td>
<td>BER₁₂</td>
<td>BER₁₆</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Upper cell data**
- **Lower cell data**
- **Left cell**
- **Right cell**
- **EP table**
- **BER**
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Acceptable Retention Time Extension

- Acceptable retention time is measured with 2 code rates (9/10, 2/3) and ECCs (BCH, EP-LDPC).

[Diagram showing retention time comparison between proposed EP-LDPC and conventional BCH, with measurement acceleration due to temperature and N_{W/E}.]
Improvement of Acceptable BER

- Acceptable BER is measured with 2 code rates (9/10, 2/3) and ECCs (BCH, EP-LDPC).

![Graph showing improvement of Acceptable BER with 2 code rates (9/10, 2/3) and ECCs (BCH, EP-LDPC).](image)
Improvement of Acceptable W/E Cycles

- Acceptable W/E cycles is measured with 2 code rates (9/10, 2/3) and ECCs (BCH, EP-LDPC).

![Graph showing improvement of acceptable W/E cycles with different code rates and ECCs at 85°C.

- Code rate: 9/10
- Code rate: 2/3

Retention time, $T_{Retention}$ (Day)

Acceptable W/E cycles, $N_{W/E}$

- Conventional BCH
- Proposed EP-LDPC

$X_{nm}$

@85 degC

Retention (Day)

x1.6

x1.5
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Flow of Error Recovery Scheme

When LDPC decoding fails...

Error mode detection

Program disturb error is dominant
\(N_{1}^{\text{initial}} > N_{1}^{\text{measured}}\)

Apply program disturb error recovery pulse (PDRP)

Data retention error is dominant
\(N_{1}^{\text{initial}} < N_{1}^{\text{measured}}\)

Apply data retention error recovery pulse (DRRP)

Read again and set as a bad block
Program Disturb Error Recovery Pulse (PDRP)

- Electrons at the interface between control gate (CG) and inter-poly dielectric (PD) are de-trapped with PDRP.
Measurement results of PDRP

- Program disturb BER is reduced by 76% by PDRP.
- The recovered data is read about 10ms after PDRP.

![Graph showing program disturb BER reduction with and without PDRP.](image)
• BER with PDRP converges to the BER without PDRP.

**Program disturb BER**

- **$N_{W/E}$**: ~20k cycles
- **3Xnm**
- **-48%**
- **~10ms**
- **Electrons are re-trapped.**
- **Explanation of detrapping mechanism.**

**Graph Details:**
- **X-axis:** Time after PDRP (ms)
- **Y-axis:** Program disturb BER
- **Legend:**
  - △ w/o PDRP (Conventional)
  - ○ w/ PDRP (Proposed)
Data Retention Error Recovery Pulse (DRRP)

- Electrons are injected to the floating gate with DRRP.
Measurement results of DRRP

- Data retention BER is reduced by 56% by 500-times DRRP.
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SSD Photograph

NAND controller  NAND flash memories

SATA controller

S. Tanakamaru et al., ISSCC, pp. 204-205, 2011.
## Summary of Key Features (1)

<table>
<thead>
<tr>
<th>Considered information</th>
<th>BCH $V_{TH}$</th>
<th>LDPC ($V_{TH}$ Soft decoding)</th>
<th>EP-LDPC $V_{TH}$ Inter-cell coupling W/E cycles Retention time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sequential read cycles</td>
<td>x1</td>
<td>x7</td>
<td>x1</td>
</tr>
<tr>
<td>Acceptable retention time</td>
<td>4 days</td>
<td>-</td>
<td>45 days (&gt;x10)</td>
</tr>
</tbody>
</table>

### Summary of Key Features (2)

<table>
<thead>
<tr>
<th>Feature</th>
<th>Conventional SSD</th>
<th>Proposed SSD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program disturb error recovery</td>
<td>None</td>
<td>PDRP (-76%)</td>
</tr>
<tr>
<td>Data retention error recovery</td>
<td>None</td>
<td>DRRP (-56%)</td>
</tr>
</tbody>
</table>

**Diagrams:**
- **PDRP** (Conventional SSD):
  - CG: 20V
  - IPD: 8V
- **DRRP** (Proposed SSD):
  - CG: 3V
  - TD: 0V
Conclusion

• Highly reliable solid-state drive (SSD) is proposed with two key techniques.
• Error-prediction (EP) LDPC architecture is proposed.
• By estimating the BER of each memory cell with the pre-recorded tables, acceptable retention time increases by over 10-times.
• Error-recovery (ER) scheme is proposed.
• Bit error is reduced by 76% with error-recovery pulses.
Thank you for your attention

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